Three-Dimensional Electrostatic Effects of Carbon Nanotube Transistors

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ABSTRACTS

We explore the three-dimensional (3D) electrostatics of planar-gate CNTFETs using a self-consistent solution of the Poisson equation with equilibrium carrier statistics. We examine the effects of the gate insulator thickness and dielectric constant and the source/drain contact geometry on the electrostatics of bottom-gated (BG) and top-gated (TG) devices. We find that the electrostatic scaling length is mostly determined by the gate oxide thickness, not by the oxide dielectric constant. We also find that a high-k gate insulator does not necessarily improve short-channel immunity because it increases the coupling of both the gate and the source/drain contact to the channel. It also increases the parasitic coupling of the source/drain to the gate. Although both the width and the height of the source and drain contacts are important, we find that for the BG device, reducing the width of the 3D contacts is more effective for improving short channel immunity than reducing the height. The TG device, however, is sensitive to both the width and height of the contact. We find that one-dimensional source and drain contacts promise the best short channel immunity. We also show that an optimized TG device with a thin gate oxide can provide near ideal subthreshold behavior. The results of this paper should provide useful guidance for designing high-performance CNTFETs.

I. INTRODUCTION

Single wall carbon nanotubes (CNTs) are of great interest for future electron device applications because of their excellent electrical properties [1-8]. Electrostatics are an important factor in transistor performance and therefore need to be carefully studied. It is well-known that the electrostatics of carbon nanotube devices can be significantly different from bulk devices due to the one-dimensional channel geometry [9, 10]. Previous theoretical studies of CNTFET electrostatics assumed a coaxial geometry [11, 12, 13]. These studies thoroughly described the role of the 2D coaxial environment on the electrostatics of the 1D channel. The coaxial geometry provides good gate control with subthreshold swings very close to 60mV/decade, and the oxide thickness and dielectric constant both play an important role by determining the gate capacitance of the device. The contact geometry also plays an important role in the transfer of charge from the metal contact to the CNT. For low Schottky barriers (SB), a large charge transfer can be achieved if the contact has a large surface area and the oxide dielectric constant is large. Thin oxides and small contact areas can achieve very short electrostatic scaling lengths (the distance by which the source and drain fields penetrate into the channel) and therefore good electrostatic behavior.

While a coaxial geometry provides important qualitative insights into the behavior of experimental devices (which typically have a planar top or bottom gated geometry), a full, three-dimensional treatment of planar devices is needed. In this work, we performed a careful study of the 3D electrostatics of planar-gated CNTFETs. Our objective is to provide both qualitative and quantitative insights valid for realistic devices. Several of the results are analogous to those that occur in a coaxial geometry, but we show

quantitatively how they play out in a realistic, planar geometry. The results should be useful for interpreting experiments and for designing high-performance CNTFETs [14].

Among the several techniques available to treat 3D electrostatics, we find the method of moments (also known as the boundary element method) well-suited for simulating planar-gate CNTFETs. This method is computationally inexpensive because it uses grid points only on the surfaces where charge exists and not in the entire 3D domain. The computational domain is thus reduced only to the important device regions, the channel, the contacts and the gate. The problem of boundary conditions in the open areas and termination of the simulation domain does not appear at all. Since all the boundary elements are assumed to be point charges, the electrostatic potential of the system decays to zero at infinity, where both potential and electric field are zero. In this way, the method of moments inherently assumes a zero-field boundary condition as the distance $r \to \infty$, which facilitates the simulation of devices with electrostatically open boundaries, (e.g. the back-gated CNTFET).

We examine the effect of the oxide thickness, the oxide dielectric constant, and the contact geometry for two different device geometries, the bottom-gated (BG) and top-gated (TG) devices shown in Fig. 1. We will show that for a CNTFET with either of these two geometries, the scaling length is mostly determined by the gate oxide thickness. The geometry of the source and drain contacts can also play an important role. The BG device is more sensitive to the contact width rather than the contact height because a wider device more effectively screens the gate field and prevents it from terminating on the CNT. We will also show that high-k dielectric materials do not offer a significant

advantage for the BG device because the oxide thickness plays the dominant role. Both the effects of contact height and high-k materials are however more pronounced for the TG device, where the high-k dielectric in the upper region increases not only the gate to CNT coupling, but also the contact to CNT coupling and the contact to gate parasitics as well. When the contacts are thick and can screen the gate field and prevent it from terminating on the channel, high-k dielectrics can actually degrade the electrostatic performance of the device. A careful geometry optimization for the contacts of planar short channel devices is, therefore, important. A properly designed TG device with very thin gate oxide can provide near ideal subthreshold behavior, similarly to what is predicted for coaxial geometries. Finally, we find that one-dimensional "needle-like" contacts offer the best electrostatic performance. In practice however, this advantage would have to be balanced against the increased series resistance.

II. APPROACH

Figures 1(a) and 1(b) show the bottom-gated and the top-gated device structures, with air (k=1) and HfO_2 (k=16) as the top region dielectric respectively. For both cases the bottom gate dielectric material is SiO_2 (k=3.9). The nominal values of the device parameters are described as follows. The thickness of the bottom gate oxide (t_{ox}) is 10nm and the width (W) of the device and of the contacts (z-direction) is 40nm. The channel length is 30nm. We assume a 10nm height for the contacts (t_c) in the air region (y-direction) and a 10nm contact length (x-direction). The geometry is similar to a recently reported CNTFET [6], except that the width of the contacts is considerably smaller, but

already wide enough for electrostatic considerations. (Making the width even larger does not change the results.) We assume a gate workfunction that produces flat band conditions at V_G = 0V ($\Phi_{Gate} = \Phi_{CNT}$), so the gate tends to keep the undoped CNT intrinsic.

For our simulations, we assume a zero Schottky barrier for electrons between the metal contacts and the nanotube, which aligns the metal Fermi level to the conduction band edge of the nanotube. Chen et al. have experimentally shown that that palladium (Pd) and titanium (Ti), commonly used metals for CNTFET contacts, form a zero barrier for holes with 2nm diameter CNTs [15]. The (25,0) CNT assumed in this study also has a diameter of 2 nm. Low Schottky barriers to the conduction band have not been reported, but the conduction and valence bands of CNTs are symmetric, so our results for electrons can be considered representative of what can be achieved in practice for holes, and the analysis on conduction band is conceptually easier to follow. For the assumed low Schottky barrier, charge transfer from metal contacts to the channel is pronounced [16]. The contacts therefore tend to "dope" the channel n-type. One might ask how our conclusions would change for larger Schottky barriers. It has been shown (for cylindrical geometries) that for large Schottky barriers, the charge transfer is reduced significantly, but at the expense of on-current reduction. We have chosen in this work to focus on the no-barrier case because it promises the highest performance.

The equilibrium band profiles were obtained by solving the Poisson equation in 3D rectangular coordinates using the method of moments [17], self consistently with equilibrium carrier statistics of the carbon nanotube [11]. The equilibrium assumption is

convenient for efficient simulation and adequate to examine the essential features of 3D electrostatics. The equilibrium charge density per unit length, Q_L(z), in the CNT is calculated by integrating the "universal" density of states (DOS) [18] over all energies,

$$Q_L(z) = -q\left(n(z)-p(z)\right)=(-q)\int_{-\infty}^{\infty} dE.\mathrm{sgn}(E).D(E).f\left[\mathrm{sgn}(E).(E-E_{Fo})\right] , \qquad (1)$$

where q is the electron charge, n(z) and p(z) are the number of electrons and holes in the CNT as a function of position, $D(E)$ is the density of states, sgn is the sign function and $E_{Fo}(z)=E_F-E_i(z)$ is the Fermi level minus the intrinsic energy of the nanotube. The Fermi level is set to zero (E_F = 0) since the source/drain contacts are grounded. The nanotube intrinsic energy is computed from the electrostatic potential at the CNT by $E_i(z)=-qV(z)-E_g/2$, where E_g is the band gap of the nanotube. The electrostatic potential $V(z)$ is taken along the axis of the CNT; we assume that the potential around the CNT circumference is close to its average potential and the charge distribution around the CNT is uniform. This assumption suggests that the modes of the CNT are decoupled and each of them can be treated individually. It is generally valid as long as the potential variation in the confinement direction (the circumference of the CNT in this case), is much less than the subband separation [19]. For a (25,0) CNT, the separation between the first and second subband is ~0.22eV. Our own more sophisticated calculations that treat the 3D variation around the CNT circumference show that even in the extreme case of a very thin gate oxide (2nm) and high gate bias (0.7V), the potential variation is 0.17V. We can, therefore, safely assume that using an average value for the potential will give accurate results.

The method of moments used to solve the Poisson equation (also known as the boundary element method) is described in [17, 20]. The charge and the potential are separated into the CNT-device (n_D, Φ_D) and the gate/source/drain-boundary (n_B, Φ_B) components. Boundary grid points are placed only where charge can reside, namely the surfaces of the source, drain and gate electrodes. The elements on the boundary surfaces are assumed to be rectangles with differential area ΔS in which the total charge is assumed to be a point charge located in the middle of the differential area. Device grid points are placed in the center of the CNT along the channel. The potential on the boundary and device is related to the charge density in the structure by:

$$\begin{Bmatrix} \Phi_D \\ \Phi_B \end{Bmatrix} = K(r; r') \begin{Bmatrix} n_D \\ n_B \end{Bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{Bmatrix} n_D \\ n_B \end{Bmatrix}, \quad (2)$$

where K is the electrostatic Kernel of the device geometry under examination partitioned into the device part (A) and the boundary part (D). The effect of charge imaging because of the different dielectric materials in the structures was also included. The potential on the device is therefore calculated from (2) to be:

$$\Phi_D = (A - BD^{-1}C)\, n_D + BD^{-1}\, \Phi_B\,. \quad (3)$$

The solution of the Poisson equation is coupled to equilibrium carrier statistics of nanotubes for calculating the charge density as described by eqn. (1), and the Newton-Ralphson method was used to improve convergence between Poisson and equilibrium carrier statistics.

III. RESULTS

A. The Bottom Gate (BG) Device.

We first examine the effect of the gate oxide thickness on the BG device shown in Fig. 1(a). Starting from the nominal device, we simulated different devices by varying the gate oxide thickness and found that this parameter has a very significant effect on the channel along its entire length. Figure 2(a) shows the effect of oxide thickness (t_{ox}) on the conduction band (E_c) of the CNT under equilibrium conditions and zero gate bias. When the channel is close to the gate, it can effectively image all of its charge on the gate metal electrode. The tube thus remains essentially intrinsic in the middle with the conduction band maximum located one-half band gap above the Fermi level ($E_g/2=0.2eV$). Our calculations show that for this case, the charge in the middle of the channel can be up to three orders of magnitude lower than the charge near the edges of the CNT, indicating a very good gate control over the channel. For the thicker gate oxides, the coupling of the gate to the channel weakens, and more field lines originating from the channel are now collected by the source/drain contacts. The relative coupling of the contacts to the channel compared to the gate coupling is now stronger. The conduction band is lowered significantly as the oxide thickness increases, and the contacts are able to inject a larger amount of charge in the channel.

Figure 2(b) shows the density of electrons in the conduction band (N_e) in units of carriers (electrons) per unit length [e/m] vs. gate bias (V_g). The electron density values are taken at a cross section in the middle of the channel for all the cases of oxide

thickness examined. In contrast to the thin oxide case, thick oxide devices are effectively doped “n-type” at low gate biases. This is a consequence of the poor carrier screening of the 1D CNT channel, enhanced by the fact that the CNT is intrinsic. As discussed in [11], this 1D screening effect is different from the case of the 2D MOSFET, in which case charge locally accumulates in the channel region directly next to the contacts. Although this study is done under equilibrium conditions, the slope of the curves in Fig. 2(b) for low gate biases is a good indication of the subthreshold current of the device. The reason is that under low gate biases, the device behaves similar to a MOSFET, where thermionic emission over the channel barrier dominates transport. For thick oxides, the subthreshold swing (*S*) is poor (well above 60mV/decade) and the density of electrons at high gate biases is low. On the other hand, better electrostatic control of the gate for thinner oxides increases the device performance by reducing *S* and increasing the electron population in the channel at high gate biases. A similar behavior for the electrostatic dependence on the oxide thickness is also observed in the coaxial device. The electrostatics of the coaxial device however, are better than those of a planar device. For the BG device, we find a subthreshold swing greater than 60mV/decade, even when the oxide thickness is 15 times less than the channel length. For a coaxial device, near ideal subthreshold swings (*S*) are possible and higher electron densities can be achieved as the gate bias increases.

Having examined the role of the bottom oxide thickness, we now consider the effect of the dielectric constant of the bottom oxide. Figure 2(c) shows the change in the conduction band profile of the nominal device, when the substrate material dielectric constant changes from air (k=1), to SiO_2 (k=3.9) to HfO_2 (k=16) and finally to ZrO_2

(k=21). Although the dielectric constant changes by a factor of 21, the effect on the device is much less than when the oxide thickness changes by a similar factor. In the case of HfO_2 and ZrO_2, the conduction band profiles are essentially identical. Figure 2(d) shows the density of electrons in the conduction band in the middle of the channel vs. gate voltage for the devices with the various dielectrics considered in Fig. 2(c). Comparing these results to Fig. 2(b), we see that a thin oxide is more effective for electrostatic gate control than an "equivalent" thicker oxide with a high-k dielectric. The subthreshold slope for the case of t_{ox}=2nm of SiO_2 (Fig. 2(b), solid-diamond line), is closer to the ideal 60mV/decade line, than for the case of the t_{ox}=10nm with a high-k dielectric device (Fig. 3(d), ZrO_2 case). In the thin oxide case, field lines from the gate can more effectively image on the channel located near by, rather than escaping toward the contacts. When the oxide is thick, however, the field lines from the gate have more chance to end up on the contacts, than on the CNT. The important point is that the electrostatics of the BG device are much more sensitive to the gate oxide thickness than to its dielectric constant.

Next, we examine how the width of the contacts (in the z-direction as shown in Fig. 1) affects the electrostatics of the BG device. We consider two cases, 5nm and 40nm contact widths. Again, the gate electrode is placed 10nm away from the channel, and the contact thickness (t_c) is 10nm. As shown in Fig. 3(a), the conduction band profile is sensitive to the width of the contacts, although this dependence is not as strong as the dependence on the gate oxide thickness shown in Fig. 2(a). There is a 20meV drop in the conduction band profile when the contact width increases from 5nm to 40nm. Figure 3(b)

shows the density of electrons in the conduction band (N_e) in the middle of the channel vs. gate bias (V_g), similar to Fig. 2(b, d). For low gate biases, wide contacts can induce a larger amount of charge in the device. As the gate bias increases, wide contacts decrease the gate coupling to the channel, and degrade the subthreshold slope of the device compared to narrow contacts.

To explain the contact width effect, we plotted in Fig. 3(c, d) the equipotential lines in an x-y cross-section taken through the center of the 3D device along the CNT channel for widths of 5nm and 40nm respectively. The source, drain, and gate are all grounded. The electrostatic potential of the source/drain is zero, and the potential of the gate is -0.21V resulting from the relative workfunction difference assumed between the gate and the source/drain electrodes. Since the CNT has very little charge at this bias, the solution of the Poisson equation is very close to the Laplace solution. In the case of the narrower contact W=5nm (Fig. 3(c)), the gate can better couple to the channel. The potential in the middle of the channel is close to -0.18V, as shown from the equipotential line just below the middle of the channel. In the case of the wide contact, W=40nm (Fig. 3(d)), the gate potential is partially screened by the contacts and its coupling to the CNT weakens. Therefore, the potential in the entire bottom region and the CNT is slightly shifted toward zero (source/drain potential), away from -0.21V (gate potential). The potential in the middle of the channel is in this case close to -0.16V, which is also reflected in the 20meV drop in E_c profile shown in Fig. 3(a).

The dimensionality of the source and drain contacts also plays an important role on the electrostatics of the BG transistor. In Figure 4(a) we plot the equilibrium conduction band profiles of three devices: 1) a device with a nanowire (1D "needle-like") contact ($W \times t_c$ = 2nm x 2nm), 2) a device with a wide but very thin (2D) contact ($W \times t_c$ = 40nm x 2nm), and 3) a device with a wide and thick (3D) contact ($W \times t_c$ = 40nm x 30nm). We find that there is minor improvement in the electrostatics when the thickness of the contact greatly decreases from 30nm (dotted line) to 2nm (dashed line). Thick contacts do not significantly affect the BG device because the contact region that affects the channel is only the part that lies within a few nanometers from the CNT. Increasing the contact height does not significantly increase its coupling to the channel because these larger contact regions are much farther away from the CNT. In addition, the tall contact surface in the upper region of the device cannot couple to the gate located in the bottom region; therefore it does not contribute to screening of the gate field either. The use of a 1D contact can improve the electrostatics of the device in agreement with [21, 22]. This improvement, however, comes mainly from the width reduction rather than the thickness reduction, as discussed in the previous section.

In order to investigate separately the screening of the channel charge by the contact alone, without the influence of the gate, we simulated a device in which the gate is placed 100nm away (more than three times the channel length). This essentially eliminates its influence on the channel. Here, the electrostatics of the device are determined by the workfunction of the nearest electrodes, the source and the drain. In Fig. 4(b) we show that due to the long range screening of the 1D channel, the conduction band

profile of the CNT along the entire channel is now lowered to 0.07eV. Once again, this behavior is observed independently of the height of the contacts. Short contacts (t_c=2nm, t_c=10nm) and tall ones (t_c=100nm) do not alter the electrostatics of the device, even in this case where the gate is far away. These results indicate that in terms of contact electrostatics of the BG device, what is of prime importance is the screening of the gate field by the contacts, as described in Fig. 3, not necessarily the overall size of the contact. For a fixed gate oxide thickness, very tall (large t_c) but thin (small W) contacts, will have less impact on the device than short (small t_c) and wide (large W) contacts. Regions of the contact that do not contribute to gate-to-contact capacitance have less impact on the electrostatics of the device.

B. The Top Gate (TG) Device

Although BG devices may find some applications, TG devices are more suitable candidates for high performance applications. In this section, we investigate the electrostatics of the top gated (TG) device shown in Fig. 1(b). The bottom gate electrode is grounded, and we apply the gate bias on the top gate electrode. For this device we find the same dependence on the oxide thickness, the oxide dielectric material and the contact geometry as for the bottom gated device. The oxide thickness (in the top region), is in this case the dominant factor controlling the electrostatic behavior of the device. In Fig. 5(a) we show that a thin top gate oxide ($tins_2$=2 nm), reduces the screening length to a few nanometers, keeping the conduction band close to the intrinsic level in most of the channel region. As the top region gate insulator thickness increases, the gate control weakens. Simultaneously the contact effect on the channel becomes stronger. The result

is a lowering of the conduction band and an increase in the subthreshold slope of the device as shown in Fig. 5(b). The TG device with a thin gate oxide (much smaller than the channel length), can result in near ideal subthreshold swings of 60mV/decade, similarly to what is observed for coaxial devices. This is an improvement over the thin oxide BG device, (Fig. 2(b)), for which the subthreshold swing deviates more from the ideal value of 60mV/decade.

Next, we examine the influence of the dielectric constant of the top region oxide. The bottom region material is still assumed to be SiO_2 (k=3.9). Figure 5(c) shows the change in the conduction band of the nominal TG device (with 10nm top and bottom oxide thickness and 10nm contact thickness) when the dielectric constant of the top region changes from air (k =1) to ZrO_2 (k =21). The variations in the conduction band are much less than when the oxide thickness changes by a similar factor. Similar trend was observed for the BG device. The main difference between the TG results in Fig. 5(c) and the BG results in Fig. 2(c) is that a lower dielectric constant is better for the TG device. One reason for this behavior is the increasingly stronger contact-to-channel coupling with increasing dielectric constant. Another reason, is that for this short channel device with relatively thick oxide, a large portion of the gate charge is more likely to image on the 2D contact surface rather than the 1D channel. The fact that the contacts are now in the same region as the top gate, makes this possible. High-k dielectric materials can enhance this parasitic coupling more than they increase the gate-to-channel coupling. As a result, the effect of the gate on the channel weakens, while the effect of the contact to the channel increases. For longer devices, and thinner oxides however, the relative contact parasitic

coupling compared to gate-to-channel coupling will be reduced, and a high-k dielectric can enhance the performance.

Figure 5(d) shows the density of electrons in the conduction band in the middle of the gate vs. gate voltage for the devices with dielectrics considered in Fig. 5(c). Although the devices with high-k dielectrics can accumulate more charge in the channel due to the enhanced contact parasitics, they have better subthreshold slopes (closer to 60mV/decade), than the low-k devices. High-k dielectric devices can be beneficial for improving subthreshold characteristics up to some degree; however a comparison to Fig. 5(b), shows that much larger subthreshold performance improvement can be achieved by reducing the oxide thickness.

Finally, we investigate the effect of the contact dimensionality on the electrostatics of the TG device. We find that the TG device is much more sensitive to contact geometry than the BG device for the same reasons discussed in the previous section. The geometry of the device allows stronger contact coupling to the gate and the channel. In Fig. 6(a) we compare the conduction band profile of the nominal TG device with a device with "needle-like" contacts, of 2nm width and 2nm thickness. In this case, the parasitic coupling of the contacts to all other device regions (top, bottom gates and channel), is minimized. The conduction band profile is raised by ~20meV compared to the nominal device case. This is a larger improvement compared to the BG "needle" contacts case of Fig. 4(a), where the improvement is ~10meV. The subthreshold swing is also clearly improved as shown in Fig. 6(b). To better illustrate the screening of the gate

field by thick contacts, in Fig. 6(c-d) we plot the electric field lines of the TG nominal device under V_g=0V and V_g=0.7V. Again, the plots are taken at a cross section in the middle of the device along the axis of the CNT. For Vg=0V, the gate electrostatic potential is lower compared to the source/drain due to their difference in workfunction. For higher gate biases, the potential of the gate becomes larger than the contact potential. In both cases, large screening takes place between the gate and the contacts. Ideally, field lines from the gate should end up on the channel and vise versa, rather than the contacts. For the Schottky-barrier CNTFET being considered here, the gate must extend across the entire nanotube, from the source to drain contact. For a MOSFET type structure, however, there would be a gap between the gate electrode and the contacts that could be filled with a material of a lower dielectric constant and reduce the contact-to-gate and contact-to-channel parasitic coupling. The MOSFET structure is therefore strongly preferred from a parasitic capacitance point of view.

IV. CONCLUSIONS

In this paper, we examined 3D electrostatic effects for planar-gate CNTFETs under equilibrium conditions. For an intrinsic CNT attached to metal contacts, we found that the gate oxide thickness plays a more important role in determining the geometric scaling length than does the oxide dielectric constant. Contact geometry also plays an important role. The most important effect of the contacts comes from the parasitic gate to source and gate to drain capacitance. For the BG device, narrower contacts result in shorter scaling length and better gate control because of their weak ability to screen the

gate field. The thickness of the contact does not play a significant role in the electrostatics of this device. For the TG device however, both the contact thickness as well as the width play an important role, because both of these dimensions can enhance the gate-to-contact capacitance. Optimizing the source and drain contact geometry is especially important for a high-k TG device because the contacts can effectively screen the gate field and couple well to the CNT channel. For both devices, 1D “needle-like” contacts will give the best performance in terms of electrostatics. Finally, we showed that a TG device with thin gate oxide can give near ideal subthreshold slope, as in the case for a coaxial device. Such behavior is difficult to achieve in the BG device.

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FIGURE CAPTIONS

Fig. 1. 2D cross sections of the devices simulated. (a) The bottom gate (BG) device with air (k=1) in the top region. (b) The top gate (TG) device with HfO_2 (k=16) in the top region. Both structures have SiO_2 (k=3.9) in the bottom region, width 40nm (in the z-direction), and contact thickness t_c=10nm. The CNT diameter is 2nm and the channel length 30nm.

Fig. 2 (a-b) The effect of the variation of the oxide thickness (t_{ox}=2, 10, 20, and 50nm) of the BG nominal structure at Vg=0V. The Schottky barrier height for electrons is zero and flat band gate conditions are assumed. (a) The conduction band profiles (E_c). (b) The electron density in the conduction band, in the middle of the nanotube for various gate biases, in units of carriers per unit length [e/m]. (c-d) The effect of the variation of the gate oxide dielectric constant of the nominal device. Cases for air (k=1), SiO_2 (k=3.9), HfO_2 (k=16), ZrO_2 (k=21) are presented. (c) The E_c profiles. (d) The electron density in the conduction band in units of carries per unit length [e/m].

Fig. 3. Plots describing the effect of the variation of the contact width (W=5, 40nm) of the three-dimensional planar bottom gate structure at V_g=0V. (a) The conduction band profiles. (b) The conduction band electron density in units of carriers per unit length [e/m], in the middle of the nanotube for various gate biases. (c) The equipotential lines at V_g=0V for a device with W=5nm (z-direction into the paper). The electrostatic potential on the source/drain is V_s=V_d=0V, and on the

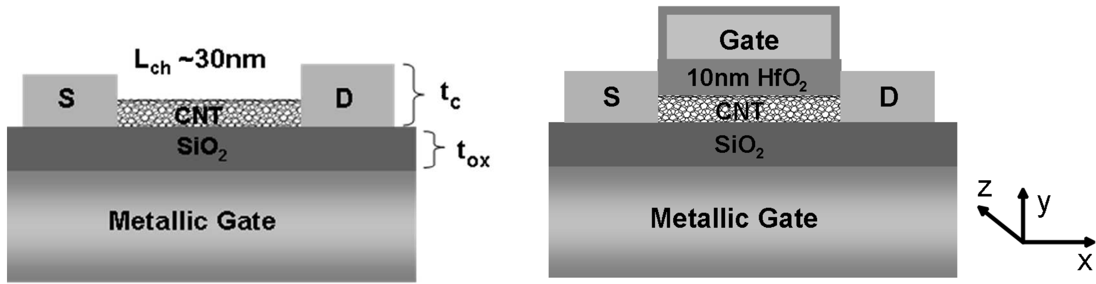
gate is -0.21V resulting from the workfunction difference between the two electrodes. (d) The equipotential lines for the case where W=40nm. The cross-section is taken in the middle of the devices on the axis along the CNT.

Fig. 4 The effect of the variation of the thickness (in y-direction) for the 3D planar BG structure. (a) The conduction band profiles for three device contact configurations with oxide thickness t_{ox}=10nm: 1) 1D contacts (2nm x 2nm), 2) wide and thin (40nm x 2nm) contacts, and 3) wide and thick (40nm x 30nm) contacts. (b) The conduction band profiles for three device contact configurations with oxide thickness t_{ox}=100nm and width W=40nm: 1) Contact height t_c=2nm, 2) t_c=10nm, and 3) t_c=100nm.

Fig. 5 (a-b) The effect of the variation of the oxide thickness ($tins_2$=2, 10, and 20nm) of the TG nominal structure at Vg=0V. The Schottky barrier height for electrons is zero and flat band gate conditions are assumed. (a) The conduction band profile (E_c). (b) The electron density in the conduction band, in the middle of the nanotube for various gate biases, in units of carriers per unit length [e/m]. (c-d) The effect of the variation of the gate oxide dielectric constant (top region oxide) of the nominal TG device. Cases for air (k=1), SiO_2 (k=3.9), HfO_2 (k=16), ZrO_2 (k=21) are presented. (c) The E_c profiles. (d) The corresponding electron density in the conduction band in the middle of the channel in units of carriers per unit length.

Fig. 6. (a) The conduction band profiles (E_c) of the TG planar device for a 3D contact with height t_c=10nm and width W=40nm, and a device with a "needle" like contact of height t_c=2nm and width W=2nm at V_g=0V. The bottom gate dielectric is k_1=3.9, and the top gate dielectric is k_2=16. The bottom gate oxide thickness is kept at $tins_1$=10nm. (b) The electron density in the E_c, in the middle of the CNT for various gate biases, in units of carriers per unit length [e/m]. (c) The electric field and equipotential lines for the zero gate bias (V_g=0V) for the TG nominal device. (d) The electric field and equipotential lines for the high gate bias case (V_g=0.7V).

FIGURE 1



(a) (b)

FIGURE 2

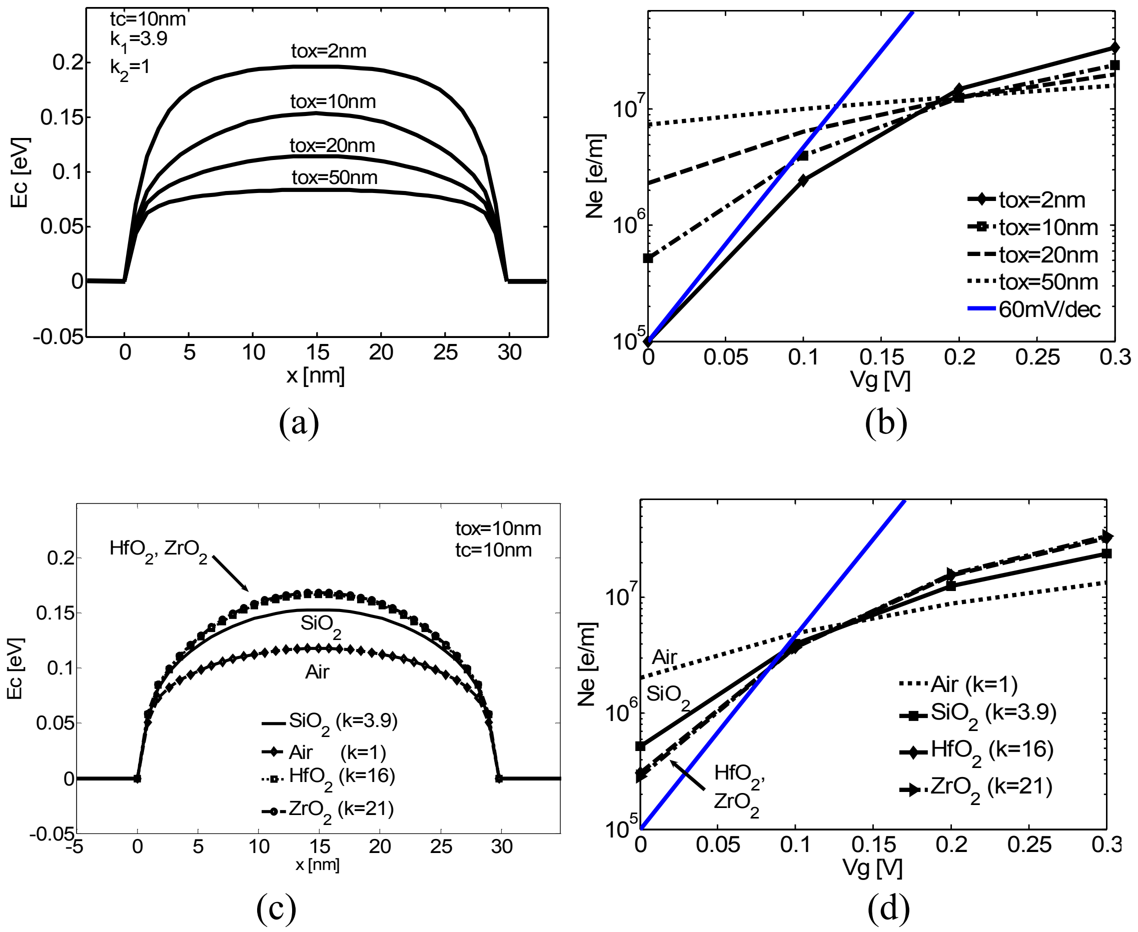


FIGURE 3

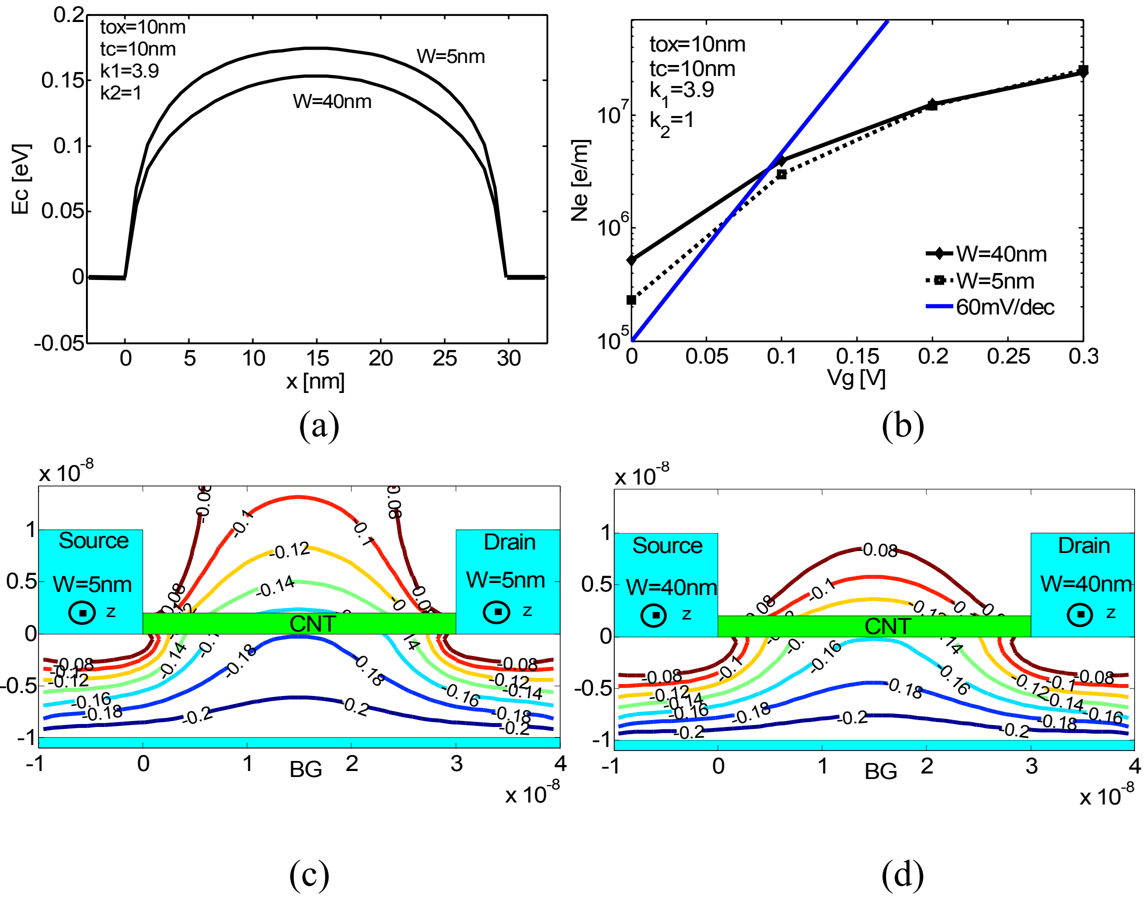
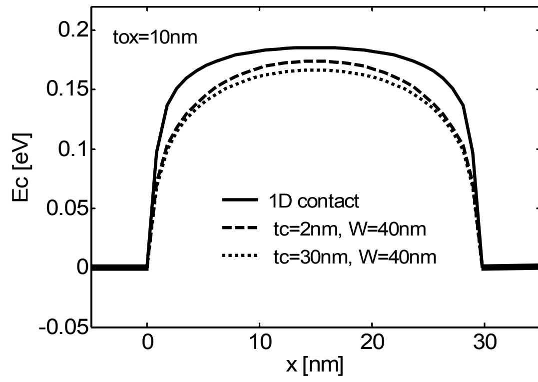
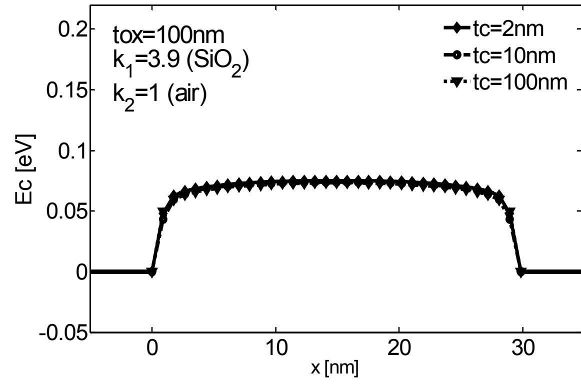


FIGURE 4



(a)



(b)

FIGURE 5

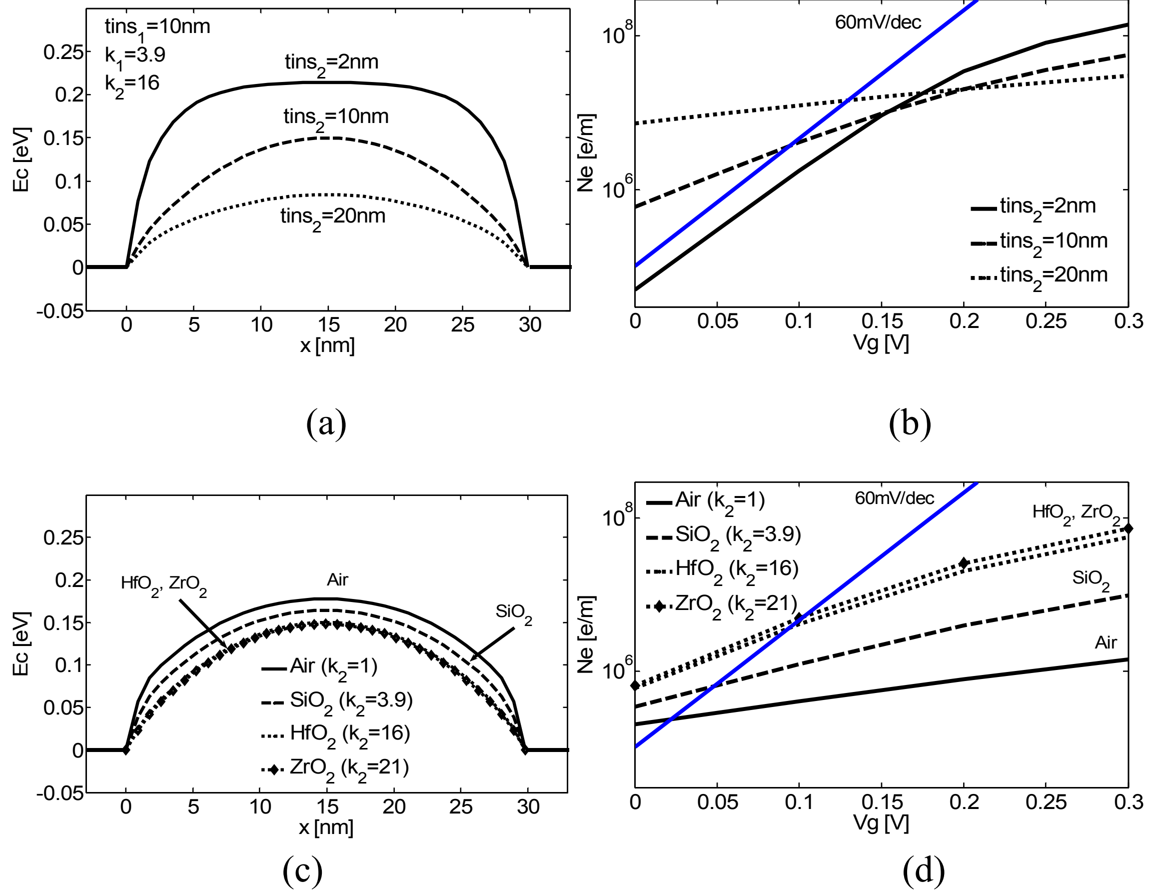
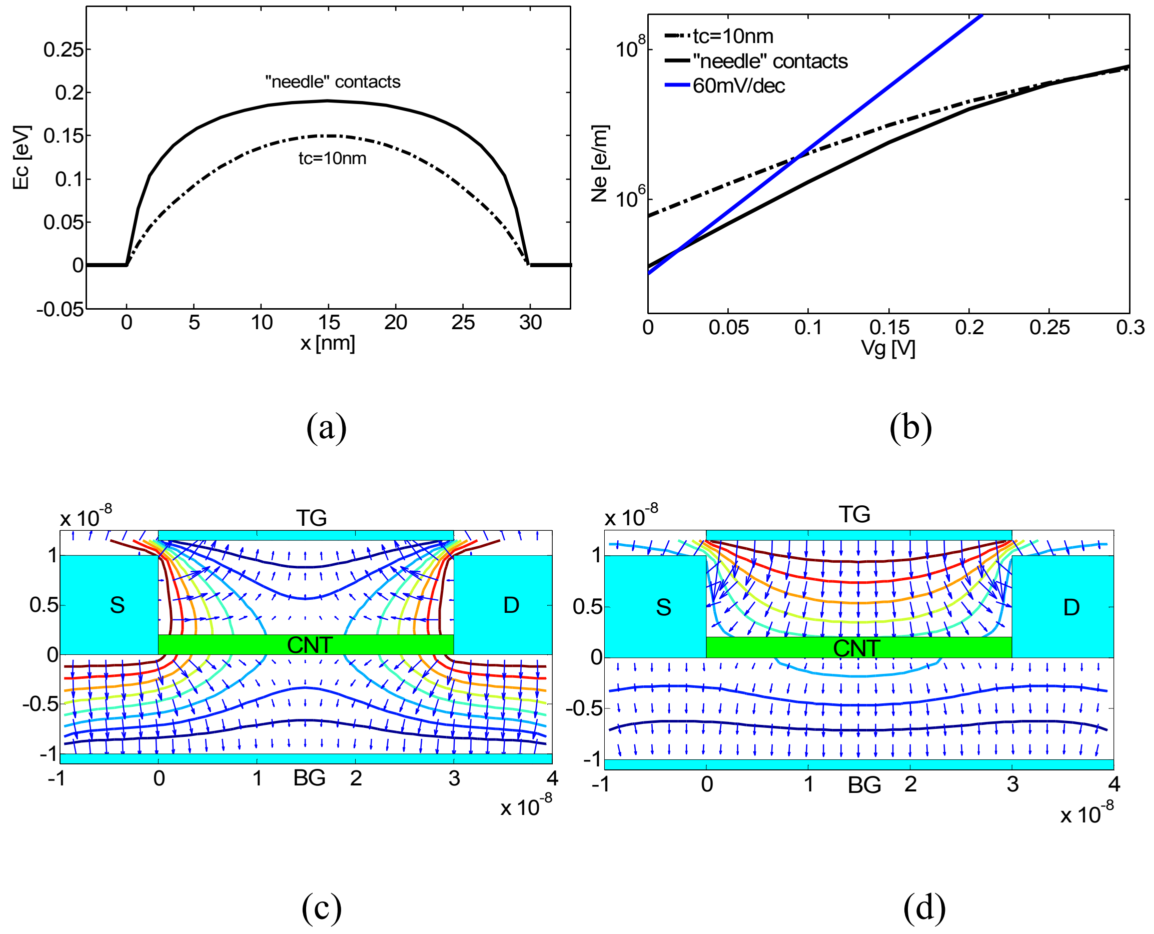


FIGURE 6



(a) (b)

(c) (d)